# Extraction Techniques for FET Switch Modeling

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***Abstract*—A new simple method for extracting equivalent circuit parameters for series and shunt GaAs FET switches is presented. The circuit elements are extracted from one set of $S$-parameter measurements for each switch state, and scale linearly with gate width. Extracted Equivalent Circuit Parameters (ECP's) are insensitive to frequency across the measured bandwidth. Good agreement has been obtained between simulated and model results for a 0.5 $\mu$m gate length series and shunt GaAs FET switches of varying gate widths, across the 0.45–26.5 GHz band.**

## I. Introduction

SERIES and Shunt GaAs FET switches are typically fabricated with a large valued gate resistor to prevent the gate bias circuitry from affecting the RF performance of the switch. The present paper approaches the modeling of GaAs FET switches from measurements made on test structures fabricated with the gate biasing resistor intact. Although much work has been done in FET characterization, previously published switch models were either based on numerical solutions or optimization [1]–[3]. While the former are theoretically rigorous in nature they are fairly complicated to apply and the correlation of produced models with measured switch behavior is unclear. Optimization based models are known to give non unique [4] and time consuming solutions. The proposed new method is an expansion on previously presented work [5] and offers an accurate, unique, and efficient solution. It is inspired by work of others in extraction based device modeling from both single [6] and several [7], [8] sets of $S$-parameter measurements. Those methods are not directly applicable with the test structures considered here, since either the gate or both gate and source cannot be RF probed. The new method is an improvement over earlier work, embodied in the inclusion of extracted intrinsic drain-to-source inductors. The method produces simple and accurate linear switch models from a single set of $S$-parameters for each switch state. Section II describes the calibration technique applied for both series and shunt devices. Section III discusses the modeling procedure for series switches. Extracted parameters and modeling results for 167, 300, and 600 $\mu$m gate width devices are presented in Section IV. Equivalent circuit extraction and modeling results for 300 and 450 $\mu$m shunt switches is discussed in Sections V–VI.

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## II. Switch $S$-Parameter Measurements

On-wafer TRL (thru-reflect-line) standards allowed establishment of accurate calibration for both the series and shunt devices prior to measuring $S$-parameters. The TRL technique is well established [9]. The on-wafer approach used here relies on coplanar waveguide-to-microstrip transition launchers connected back-to-back (thru standard), via hole grounded shorts (reflect standard) and a short delay line inserted between the transition launchers (line standard) to establish calibration referenced to the center of the thru line. Fig. 1 shows layouts of both on-wafer standards and a series switch. The TRL procedure automatically de-embeds the coplanar waveguide to microstrip transitions from measured $S$-parameters providing a reference plane at the center of the thru line standard. Thus it allows an accurate characterization of the intrinsic series FET switch shown in Fig. 1

$$\beta \times \Delta L = [(360 \times f \times \sqrt{\epsilon_{\text{eff}}})/c] \times \Delta L \qquad (1)$$

The accuracy of the TRL procedure in a particular bandwidth is dependent on the delay line length. Equation (1) shows the relation between insertion phase and frequency. For the Hewlett-Packard recommended 20–160 degrees insertion phase [10], the most accurate frequency range for the 1800 $\mu$m delay line is from 3.18–25.4 GHz. An approximate effective relative dielectric constant of 8.5 was used for the 100 $\mu$m wide microstrip lines on a 150 $\mu$m thick GaAs substrate, in the phase calculations. Another effect, not considered here, that may affect the low frequency measurements is the low frequency dispersion of the microstrip characteristic impedance [11].

## III. Series Switch Modeling Procedure

### A. Insertion Loss State

The series switch layout and equivalent circuit representation are shown in Fig. 1. Note the isolation resistor between each of the DC probe pads and the gate fingers. In switching operation, drain bias is not applied and a bidirectional RF path is formed between the drain and source. Low insertion loss is obtained by zero biasing the device ($V_{ds} = V_g = 0$). The four element equivalent circuit [Fig. 1(a)] represents the insertion loss state as a resistor in series with a channel inductance. Additional parasitic elements are included in the form of drain-to-gate and source-to-gate capacitances. Gate capacitances do not have a significant insertion loss effect yet they provide additional accuracy in modeling the input and output reflection coefficients.

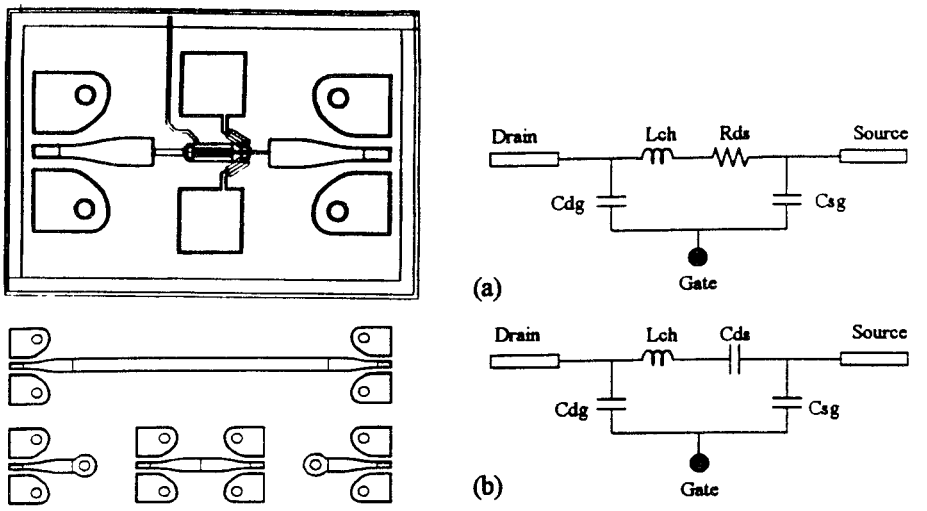


Fig. 1. TRL Calibration standards, layout and small signal equivalent circuit for a series switch insertion loss (a) and isolation (b) states.

The analysis is done in the following four steps:

1) De-embed the microstrip lines between the TRL launchers and the active device from the measured $S$-parameter file.
2) Convert the $S$-parameters of the de-embedded file to $Y$-parameters.
3) Extract the four ECP's ($L_{ch}, R_{ds}, C_{dg}$, and $C_{sg}$) from the $Y$-parameters file.
4) Embed the extracted ECP's between microstrip lines and compare model $S$-parameters with measured data.

The four element equivalent circuit can be described by the following $Y$-parameters

$$Y_{11} = \frac{1 - \omega^2 C_{dg} L_{ch} + j\omega C_{dg} R_{ds}}{R_{ds} + j\omega L_{ch}} \tag{2}$$

$$Y_{22} = \frac{1 - \omega^2 C_{sg} L_{ch} + j\omega C_{sg} R_{ds}}{R_{ds} + j\omega L_{ch}} \tag{3}$$

$$Y_{21} = Y_{12} = \frac{1}{R_{ds} + j\omega L_{ch}}. \tag{4}$$

Expressions for $L_{ch}$ and $R_{ds}$ are directly obtained from the real and imaginary parts of (4). A unique solution for $C_{dg}$ and $C_{sg}$ is obtained by substituting from (4) into (2) and (3). The following relations result

$$C_{dg} = \mathrm{Im}\left(\frac{-Y_{11}}{Y_{21}}\right) \Big/ \omega\, \mathrm{Re}\left(\frac{-1}{Y_{21}}\right) \tag{5}$$

$$C_{sg} = \mathrm{Im}\left(\frac{-Y_{22}}{Y_{21}}\right) \Big/ \omega\, \mathrm{Re}\left(\frac{-1}{Y_{21}}\right). \tag{6}$$

### B. Isolation State

A similar analysis method is used for the isolation state. Drain-to-source isolation is obtained by biasing the gate between pinchoff and breakdown ($V_{ds} = 0, V_g < V_p$). The four element equivalent circuit represents the channel [Fig. 1(b)] as a capacitor in series with a channel inductance obtained at the insertion loss state. Different, parasitic, drain-to-gate and source-to-gate capacitances are also extracted to provide improved fit to the input and output reflection coefficient. Attempts to include a large value resistor in parallel with the drain-to-source capacitor causes significant deviation in the isolation phase response at low frequency. The four element equivalent circuit can be described by the following $Y$-parameters

$$Y_{11} = j\omega\left[C_{dg} + \frac{C_{ds}}{1 - \omega^2 L_{ch} C_{ds}}\right] \tag{7}$$

$$Y_{22} = j\omega\left[C_{sg} + \frac{C_{ds}}{1 - \omega^2 L_{ch} C_{ds}}\right] \tag{8}$$

$$Y_{12} = Y_{21} = -j\omega\left[\frac{C_{ds}}{1 - \omega^2 L_{ch} C_{ds}}\right]. \tag{9}$$

With $L_{ch}$ extracted at the insertion loss state, an expression for $C_{ds}$ is obtained from the imaginary part of (9). A unique solution for $C_{dg}$ and $C_{sg}$ is then derived by substituting from (9) into (7) and (8). The following relations result

$$\frac{1}{C_{ds}} = -\frac{\omega}{\mathrm{Im}(Y_{21})} + \omega^2 L_{ch} \tag{10}$$

$$C_{dg} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{21})}{\omega} \tag{11}$$

$$C_{sg} = \frac{\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{21})}{\omega}. \tag{12}$$

## IV. Series Switch Modeling Results

Several types of switches were measured to verify the extraction procedure. Figs. 2–3 show extracted parameters for a 0.5 $\mu$m series switch of varying gate widths (167, 300, and 600 $\mu$m). The extracted parameters are frequency insensitive and can be extracted anywhere across the 3–26.5 GHz range, or obtained as an average over this bandwidth. Channel inductance, Fig. 2, is dependent on the single unit gate width used and varies from 43–57 pH for the 75 $\mu$m unit gate width devices to 65–77 pH for the 150 $\mu$m devices. Low frequency dispersion in inductance values can be attributed to the validity of the TRL calibration below 3 GHz. Insertion loss state drain-to-source resistance, Fig. 2, decreases with larger gate width and varies between 12.2 and 3.5 $\Omega$ Isolation state

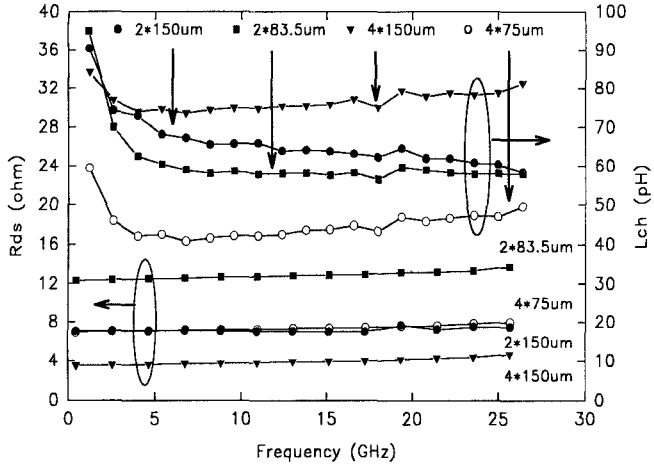


Fig. 2. Extracted drain-to-source resistance ($R_{ds}$) and channel inductance ($L_{ch}$) versus gate periphery for series switch in insertion loss state.

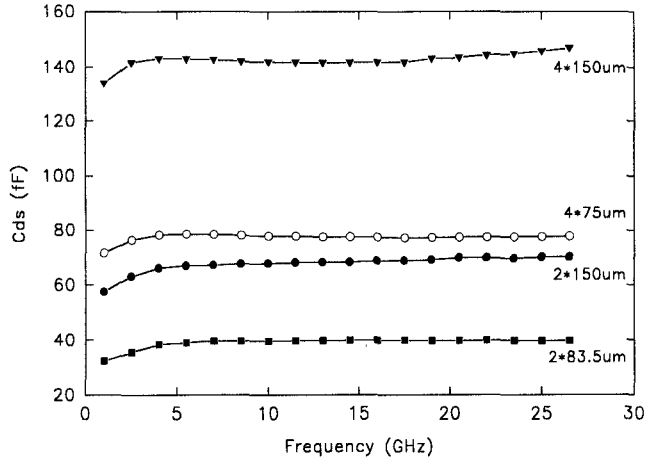


Fig. 3. Extracted drain-to-source capacitance ($C_{ds}$) versus gate periphery for series switch in isolation state.

TABLE I
EXTRACTED CHANNEL PARAMETERS VERSUS GEOMETRY FOR A SERIES SWITCH, INDICATING GATE WIDTH SCALING OF ELEMENT VALUES

| Gate Periphery | 167μm 2 fingers | 300μm 2 fingers | 300μm 4 fingers | 600μm 4 fingers | Units |
|---|---|---|---|---|---|
| Lch | 57 | 65 | 43 | 77 | pH |
| Rds | 12.2 | 7 1 | 7 1 | 3.5 | Ω |
| (Rds) x W | 2037 | 2130 | 2130 | 2100 | Ω-μm |
| Cds | 40 | 70 | 78 | 145 | fF |
| Cds / W | 0 2395 | 0 2333 | 0 2600 | 0 2416 | fF/μm |

drain-to-source capacitance, Fig. 3, increases with larger gate width from 40 fF for 167 $\mu$m to 142 fF for 600 $\mu$m devices.

Next the scaling of model elements with gate width is considered. The extracted parameters, summarized in Table I, show consistent values per micron of gate width for the drain-to-source resistance and capacitance. Small variations were observed in the shunt capacitors values. Both the drain-to-gate and source-to-gate capacitors do not scale linearly with gate width, using constant values of 25 fF for $C_{dg}$ and 10 fF for $C_{sg}$ seem to give good results for all the devices at both states.

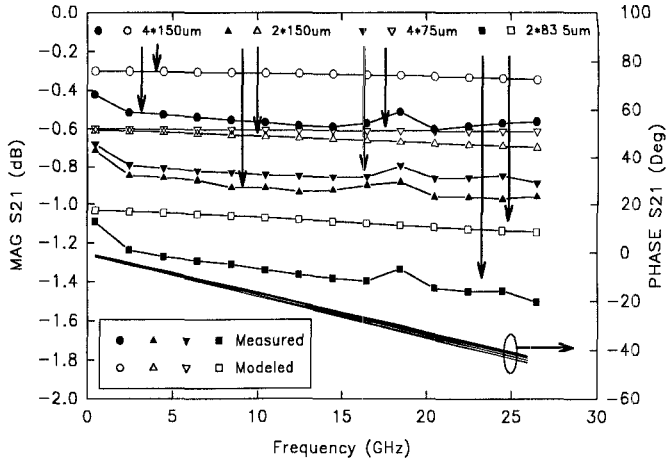


Fig. 4. Series switch performance: measured (filled) versus modeled (hollow) insertion-loss magnitude and phase response for various gate peripheries.

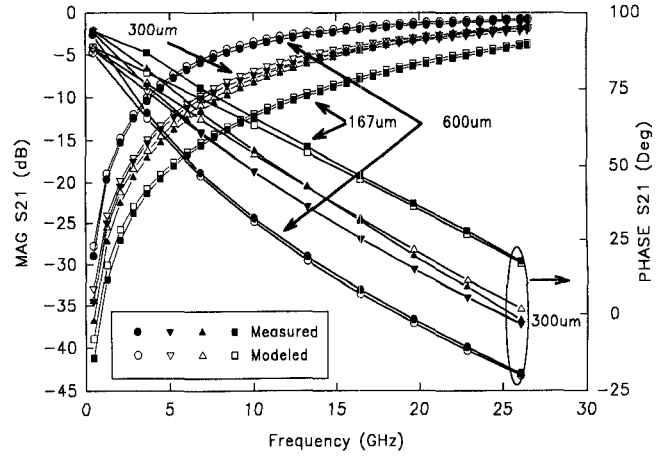


Fig. 5. Series switch performance: measured (filled) versus modeled (hollow) isolation magnitude and phase response for various gate peripheries.

Figs. 4 and 5 shows agreement between modeled and measured $S$-parameters achieved for various gate width devices across the 0.45–26.5 GHz range. Generally, larger gate width devices show better insertion loss performance at the expense of reduced isolation characteristics. Fig. 4 shows measured and modeled insertion loss magnitude and phase of $S_{21}$. Variations in insertion loss, ranging from 0.6 dB for 600 $\mu$m to 1.6 dB for 167 $\mu$m are modeled to a 0.25 dB accuracy. An accurate modeling was also obtained {for the device insensitive insertion loss state constant phase response ($-45°$ at 26.5 GHz). Isolation state magnitude and phase response are shown in Fig. 5. The 600 $\mu$m devices isolation varies from 28 to 1 dB, while 167 $\mu$m devices varies from 40 to 4 dB across the frequency range. Good agreement is shown in both the phase and magnitude $S_{21}$ for all the devices considered here.

## V. SHUNT SWITCH MODELING PROCEDURE

### A. Isolation State

A shunt switch layout and equivalent circuit model for the on and off states is shown in Fig. 6. Shunt switches are fabricated around a microstrip drain line. DC probes are used

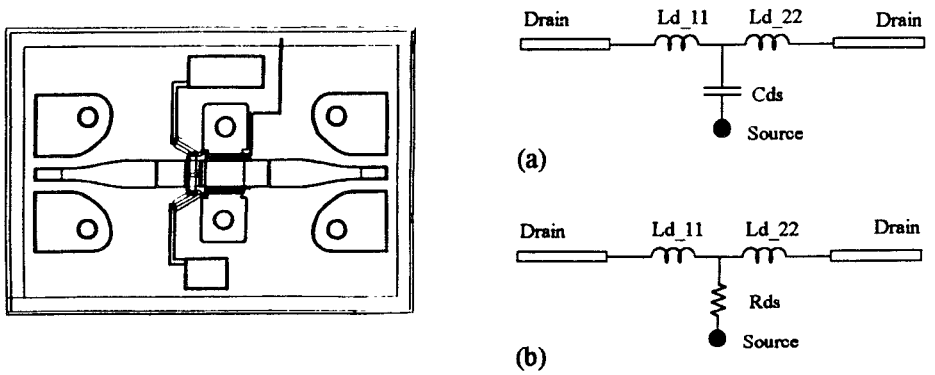


Fig. 6. Layout and small signal equivalent circuit for a shunt switch insertion loss (a) and isolation (b) states.

to bias the gate fingers which connect the drain to the via hole grounded source. The biasing for the shunt switch is opposite that for the series devices, and the on insertion loss state is obtained by pinching off the gate. The channel is modeled as either capacitive or resistive at the switch insertion loss and isolation states, respectively. Attempts at including a parallel combination of resistor and capacitor resulted in no improved fit to measured data [12].

An analysis method similar to that used for series switches was implemented to derive an equivalent circuit for the shunt switch. The intrinsic circuit can be represented in $Z$-parameters using relatively simple equations

$$Z_{ii} = R_{ds} + j\omega L_{d\_ii} \tag{13}$$

$$Z_{ig} = R_{ds}. \tag{14}$$

Resistance can be extracted from the real part of either $Z_{ij}$ or $Z_{ii}$. Using the $ij$ components produces frequency insensitive values up to 26.5 GHz, while the $ii$ components had significant deviation with frequency. Two drain inductors ($L_{d11}$ and $L_{d22}$) are extracted from (13) to model both the input ($L_{d11}$) and output ($L_{d22}$) phase response.

### B. Insertion Loss State

A similar analysis method was applied for the insertion loss state. The shunt switch insertion loss state is obtained by biasing the gate between pinchoff and breakdown ($V_{ds} = 0, V_g < V_p$). The three element equivalent circuit represents the channel as a shunt capacitor connected to two series drain inductors and is described by the following $Z$-parameters:

$$Z_{ii} = \frac{1 - \omega^2 L_{d\_ii} C_{ds}}{j\omega C_{ds}} \tag{15}$$

$$Z_{ig} = \frac{1}{j\omega C_{ds}}. \tag{16}$$

Drain-to-source capacitance is obtained from (16), inductances are best extracted at the isolation state, in which the structure is resistive.

## VI. Shunt Switch Modeling Results

Shunt switches of various gate widths were measured to verify the extraction procedure. Figs. 7 and 8 shows extracted parameters for a 0.5 $\mu$m by 300 and 450 $\mu$m.

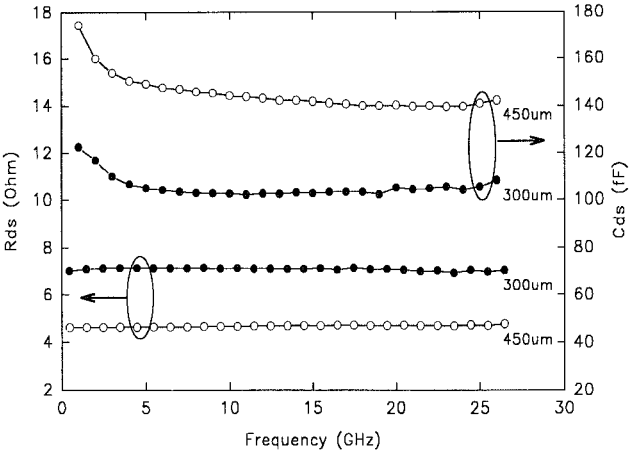


Fig. 7. Extracted drain-to-source resistance ($R_{ds}$) and capacitance ($C_{ds}$) versus gate periphery for a shunt switch.

The extracted parameters are frequency insensitive and can be extracted anywhere across the 3–26.5 GHz bandwidth, or averaged over this band. Isolation state drain-to-source resistance, Fig. 7, decreases with larger gate width and varies between 7.1 Ω (300 $\mu$m) and 4.7 Ω (450 $\mu$m). Insertion loss state drain-to-source capacitance, Fig. 7, increases with larger gate width from 104 fF (300 $\mu$m) to 142 fF (450 $\mu$m). Drain inductance, Fig. 8, is extracted from both the input and output port. Typically, inductance is dependent on the single unit gate width used, and varies from 15–20 pH for the 150 $\mu$m unit gate width devices to 33–40 pH for the 225 $\mu$m devices. The extracted parameters, summarized in Table II, show consistent values per micron of gate width for both $R_{ds}$ and $C_{ds}$.

Figs. 9–10 shows agreement between modeled and measured $S$-parameters achieved for various gate width devices across the 0.45–26.5 GHz range. Generally, smaller gate width devices show better insertion loss performance at the expense of reduced isolation characteristics—opposite to the trend observed in series devices. Fig. 9 shows measured and modeled insertion loss state magnitude and phase of $S21$. Variations in insertion loss, ranging from 0–0.6 dB for 300 $\mu$m and 0–1 dB for 450 $\mu$m are modeled to an accuracy of 0.15 dB across the measured bandwidth. An accurate modeling was also obtained for the various devices' phase shift ($-60°$ at 26.5 GHz). Isolation state magnitude and phase response are shown in Fig. 10. Unlike series devices, shunt switches have constant isolation with frequency. The 300 and 450 $\mu$m devices have

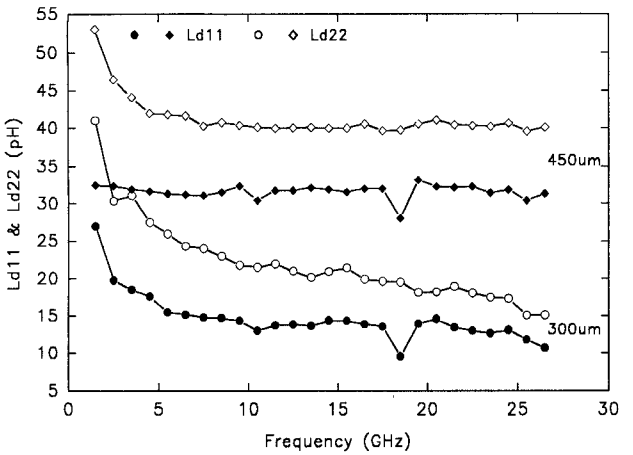


Fig. 8. Extracted input and output drain inductance ($L_{d11}$ and $L_{d22}$) versus gate periphery for a shunt switch.

TABLE II
EXTRACTED PARAMETERS VERSUS GEOMETRY FOR A SHUNT SWITCH, INDICATING GATE WIDTH SCALING OF ELEMENT VALUES

| Gate periphery | 300μm 2 fingers | 450μm 2 fingers | Units |
|---|---|---|---|
| Ld11 | 15 | 33 | pH |
| Ld22 | 20 | 40 | pH |
| Rds-off | 7 1 | 4 7 | Ω |
| Rds-off × W | 2130 | 2115 | Ω-μm |
| Cds-on | 104 | 142 | fF |
| Cds-on / W | 0 3466 | 0.3155 | fF/μm |

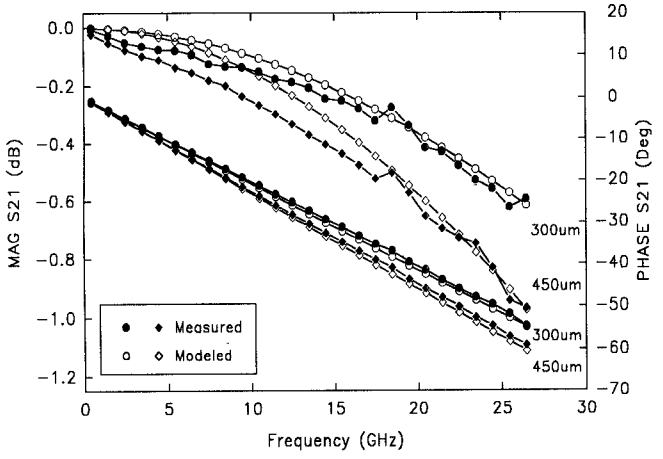


Fig. 9. Shunt switch performance: measured (filled) versus modeled (hollow) insertion-loss magnitude and phase response for various gate peripheries.

isolations of 13 and 16 dB, respectively. Good agreement is shown in both the phase and magnitude $S21$ for all the devices considered here.

The presented techniques were employed to obtain temperature dependent series and shunt switch models over a broad (25−125°C) temperature range [12]. Predominantly linear variations were observed in the channel resistance and capacitance of the six devices. Inductance values which are highly sensitive to probe placement repeatability and wafer thermal expansion, were found to be best held at their room temperature values. Typical resistance variations over a 100°C range were less than 1. Capacitance variations, over the same range,

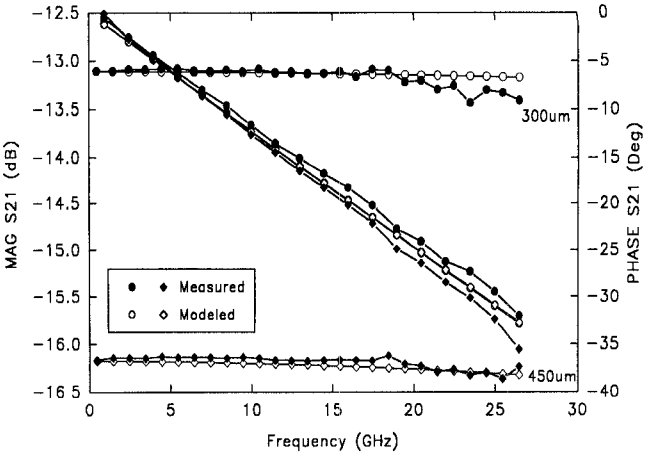


Fig. 10. Shunt switch performance: measured (filled) versus modeled (hollow) isolation magnitude and phase response for various gate peripheries.

were less than 15 fF. Investigating the switches' sensitivity to temperature variations shows slight performance degradation with increasing temperature. Increases in series switch insertion-loss (with temperature increase) of four gate finger FETs (0.06 dB) were smaller than the increased insertion-loss observed for two gate finger devices (0.2 dB). Shunt switch degradations in isolation of about 0.8 dB were observed. No significant degradation occurred in either series switch isolation or shunt switch insertion-loss. Overall, the effect of temperature on linear FET switch behavior while not dramatic, can be modeled with the extraction techniques described herein.

## VII. CONCLUSION

A simple and efficient extraction method for GaAs FET switches was developed. The commonly used hot/cold techniques for FET modeling are not applicable with gate bias isolated switches since the gate cannot be RF probed. Extraction based equivalent circuit models presented for shunt and series switches are superior for applications such as temperature dependent modeling where uncertainties in optimization routines may fail to predict changes in device parameters. The model can also be useful for characterizing the affect of process variations such as gate width, length and metalization thickness. Good measured to modeled data fit was obtained across the 0.45–26.5 GHz bandwidth for all devices considered here.

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